REMARKS

Claims 28-29, 33, 35, and 37-39 are currently pending in the present application. Reconsideration and reexamination of the claims are respectfully requested.

Applicants express appreciation for the Examiner's time in conducting a telephonic interview for this case on June 27, 2006.

The Examiner rejected the pending claims under 35 U.S.C. § 103(a) as being unpatentable over Applicants' admitted prior art (as shown in Fig. 1 of the present application) in view of Baskett (U.S. patent no. 6,333,672). This rejection is respectfully traversed with respect to the pending claims.

The present invention is directed to a high speed, high resolution digital to analog converter (DAC). Specifically, with reference to Fig. 3 of the present application, a plurality of cascode current output block 52 is used as a unitary switching element (e.g., a unit cell) of a DAC. This is in contrast to the conventional differential pair switching element such as 12 and 14 shown in the DAC of Fig. 1 of the present application.

Claim 28 is directed generally to Fig. 3 of the present application. Specifically, Claim 28 recites a DAC having a first and second summing bus (e.g., 16 & 18 in Fig. 3), a plurality of current switch cells (e.g., 52), each of which includes a first current source (e.g., 20 in Fig. 3) for supplying a first current, a pair of differential transistors (e.g., Q1 & Q2 in Fig. 3), a pair of cascode transistors (e.g., Q_A and Q_B in Fig. 3) having emitters respectively coupled to the collectors of Q1 and Q2 and collectors coupled to the first and second summing buses, and two additional current sources for supplying trickle currents to the emitters of the cascode transistors (e.g., 56 & 58 in Fig. 3). The use of the cascode circuits with trickle currents as unit cells in a DAC improves the performance of the

DAC by providing a faster overall operating speed and improved accuracy, while eliminating parasitic capacitance (a.k.a. Miller effect) typically associated with convention DAC architecture using transistors that do not apply the principle of using trickle currents.

The Examiner has rejected the pending claims as being obvious in view of Fig. 1 of the present application in view of Baskett. Applicants respectfully submit that, even when combined, the references do not show the claimed invention.

Fig. 1 of the present application illustrate a conventional implementation of a DAC. As described in page 4 of the present application, DAC 10 includes a plurality of cells (12, 14) each of which includes a current source (20, 22) and a pair of differential transistors (Q1, Q2 and Q3, Q4). The DAC includes summing buses (16, 18) connected to ground via load resistance R_L. Fig. 1 of Baskett, on the other hand, illustrate a differential logic circuit for providing pure digital output (i.e., Fig. 1 of Baskett is not directed to a DAC).

Applicants respectfully submit that the admitted prior art, even when combined with Baskett, do not contain any disclosure or suggestion of the DAC recited in Claim 28. Specifically, the admitted prior art does not contain any disclosure of cascode transistors or trickle current sources, as recited in Claim 28. Baskett fails to make up for this deficiency. In particular, although Fig. 1 of Baskett shows transistors 16 and 18 for providing nominal current to "keep alive" the transistors 12 and 14, there is no teaching or suggestion of incorporating the structure shown in Baskett into the DAC shown in Fig. 1 of the present application. And, more specifically, there is no teaching or suggestion of connecting the emitters of a pair of cascode transistors to collectors of differential pair transistors, as recited in Claim 28.

In further regard, the Examiner does not point to any teaching or motivation, on either the admitted prior art or Baskett, for combining the two references. Specifically, there is no motivation for combining circuitry of a differential logic gate, used for digital output purposes and having only two digital outputs of high and low, into a circuitry of multiple switching cells for outputting analog outputs of various resolutions. Again, Applicants note that discussions of Fig. 1 in the present application is NOT prior art itself.

As it is well known in the art, there exist many different types of current switches in electrical applications, just as there exist numerous different electrical elements generally. It is well recognized that a novel combination of elements, even if the elements are known in the art, is patentable. See, e.g., In re Lunsford, 357 F.2d 380, 384 (C.C.P.A. 1966) (citing In re Wright, 268 F.2d 757 (C.C.P.A. 1959). At the same time, it is also well settled patent law that hindsight cannot be used as motivation for combining prior art references. See, e.g., Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1139 (Fed. Cir. 1985) (vacating judgment by trial court, noting it is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's claim as a "blueprint.") (citing Kalman v. Kimberly-Clark Group, 713 F.2d 760, 774 (Fed. Cir. 1983), cert denied 465 U.S. 1026 (1984)). Rather, there must exist some suggestion, teaching, or motivation that would have led a person of ordinary skill in the art to combine the prior art references in a manner claimed. See Graham v. John Deere Co., 383 U.S. 1 (1966); In re Dembiczak, 175 F.3d 994, 998 (Fed. Cir. 1999). To do otherwise, "combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability -- the essence of hindsight." Dembiczak, 175 F.3d at 999. In this regard, the Federal Circuit has consistently held that a person of ordinary skill

in the art "must not only have had some motivation to combine the prior art teachings, but some motivation to combine the prior art teachings in the particular manner claimed." Teleflex Inc. v. KSR Int'l Co., 119 Fed. Appx 282 (Fed. Cir. 2005) (citing In re Kotzab, 217 F.3d 1365, 1371 (Fed. Cir. 2000) ("Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed.")).

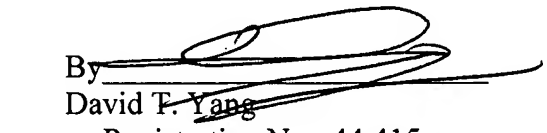
With respect to the motivation for combining the references, the Examiner simply states that "the discussion by Baskett of the benefits of [trickle] transistors (thus providing the motivation for one of ordinary skill in the art to add such cascode transistors and trickle current sources to the circuitry shown in [Fig. 1 of the present application]." Applicants respectfully submit that the Examiner's observations are not supported by the references. In fact it wouldn't make any sense, from a digital logic perspective as taught by Baskett, to construct multiple [>2] logic states by incorporating the circuit shown in Fig. 1 of Baskett with that of Fig. 1 of the present application. Again, Applicants respectfully submit that the Examiner appears to have been influenced by the pending claims as a foundational blueprint and, in hindsight, reconstructed the claimed invention by selectively combining the references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 535352003600.

Dated: June 28, 2006

Respectfully submitted,



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